PYRAMID SEMICONDUCTOR CORPORATION

PY29F040

512K x 8 FLASH

UNIFORM SECTOR 5.0V FLASH MEMORY

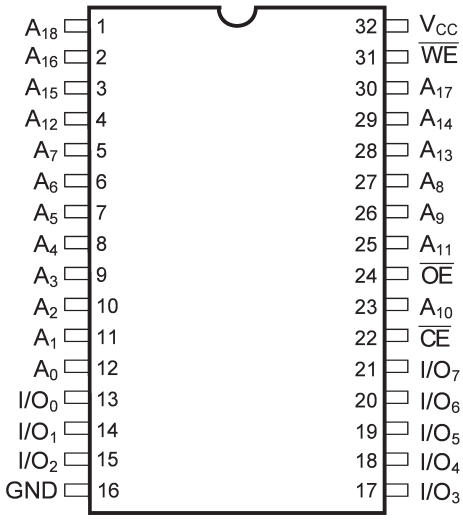
FEATURES

- **Single 5V±10% Power Supply**
- **Fast Access Time: 55ns**
- **Low Power Consumption**
  - **20 mA typical active read current**
  - **30 mA typical program/erase current**
  - **1 µA typical standby current (standard access time to active mode)**
- **Flexible Sector Architecture**
  - **Eight uniform 64 Kbyte each**
  - **Any combination of sectors can be erased**
  - **Supports full chip erase**
- **Sector protection**
- **Embedded Algorithms Erase & Program Algorithms**
- **Erase Suspend/Resume**
- **Minimum 100,000 Program/Erase Cycles per sector guarantee**
- **Compatible with JEDEC standards**
  - **Pinout and software campatible with single power supply FLASH**
- **$\overline{\text{DATA}}$ Polling and Toggle Bits**
- **20-year data retention at 125°C**

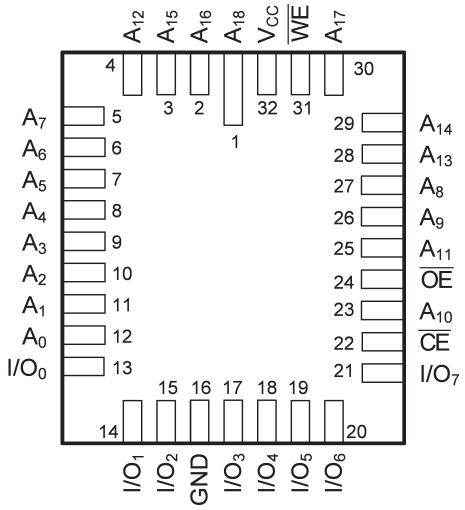
OPTIONS

- **Speed: 55/60/70/90/120/150 ns**
- **Temperature:**
  - **Commercial (0°C to +70°C)**
  - **Industrial (-40°C to +85°C)**
  - **Military (-55°C to +125°C)**
  - **QML processing (-55°C to +125°C)**
- **Packages:**
  - **Ceramic DIP**
  - **LCC**
  - **Flatpack**

PIN ASSIGNMENT



(Top View)
32-pin Ceramic DIP (CW)
32-pin Flatpack (FS)



32-pin LCC (L)

GENERAL DESCRIPTION

The PY29F040 is a 5.0 volt-only Flash memory organized as 524,288 bytes of 8 bits each. The 512 Kbytes of data are further divided into eight sectors of 64 Kbytes each for flexible sector erase capability. The 8 bits of data appear on I/O_0 - I/O_7 while the addresses are input on A_0 to A_{18}. The PY29F040 is offered in 32-pin ceramic DIP, Flatpack and LCC packages.

This device is designed to be programmed in-system with the standard system 5.0 volt VCC supply. Additional 12.0 volt VPP is not required for in-system write or erase operations. However, the PY29F040 can also be programmed in standard EPROM programmers. The PY29F040 has a second toggle bit, I/O_2, to indicate whether the addressed sector is being selected for erase, and also offers the ability to program in the Erase Suspend mode. The standard PY29F040 offers access times of 55 ns, allowing high-speed microprocessors to operate without wait states.

To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable (WE) and output enable ($\overline{OE}$) controls. The device requires only a single 5.0 volt power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. The PY29F040 is entirely software command set compatible with the JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations.

Reading data out of the device is similar to reading from other Flash or EPROM devices. Device programming occurs by writing the proper program command sequence. This initiates the Embedded Program algorithm - an internal algorithm that automatically times the program pulse widths and verifies proper program margin.

Device erasure occurs by executing the proper erase command sequence. This initiates the Embedded Erase algorithm - an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper erase margin. The host system can detect whether a program or erase operation is complete by reading the I/O_7 (Data Polling) and I/O_6 (toggle) status bits.

After a program or erase cycle has been completed, the device is ready to read array data or accept another command. The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The PY29F040 is fully erased when shipped from the factory. The hardware sector protection feature disables operations for both program and erase in any combination of the sectors of memory. This can be achieved via programming equipment. The Erase Suspend feature enables the user to put erase on hold for any period of time to read data from, or program data to, any other sector that is not selected for erasure. True background erase can thus be achieved. Power consumption is greatly reduced when the device is placed in the standby mode.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	-55°C to + 125°C
Storage Temperature	-65°C to + 150°C
V_{CC} to Ground	-2.0V to 7.0V
Output Voltage (Note 1)	-2.0V to 7.0V
A_9 & $\overline{OE}$ (Note 2)	-2.0V to 14V
All other pins (Note 1)	-2.0V to 7.0V

V_{CC} for ± 10% devices	+4.5V to +5.5V

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot V_{SS} to -2.0V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V_{CC} +0.5V. During voltage transitions, outputs may overshoot to V_{CC} +2.0V for periods up to 20ns.
2. Minimum DC input voltage on A_9 pins is -0.5V. During voltage transitions, A_9 and $\overline{OE}$ may overshoot V_{SS} to -2.0V for periods of up to 20ns. Maximum DC input voltage on A_9 and $\overline{OE}$ is +12.5V which may overshoot to 13.5V for periods up to 20ns.
3. No more than one output is shorted at a time. Duration of the short circuit should not be greater than one second.

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification in not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1 - PY29F040 Device Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0-A_{18}	I/O_0-I/O_7
Read	L	L	H	A_{IN}	D_{OUT}
Write	L	H	L	A_{IN}	D_{IN}
CMOS Standby	V_{CC} ± 0.5V	X	X	X	High-Z
TTL Standby	H	X	X	X	High-Z
Output Disable	L	H	H	X	High-Z

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5V, X=Don't Care, D_{IN}=Data In, D_{OUT}=Data Out, A_{IN}=Address In

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the $\overline{CE}$ and $\overline{OE}$ pins to V_{IL}. $\overline{CE}$ is the power control and selects the device. $\overline{OE}$ is the output control and gates array data to the output pins. $\overline{WE}$ should remain at VIH all the time during read operation. The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered. See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms, I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive $\overline{WE}$ and $\overline{CE}$ to V_{IL}, and $\overline{OE}$ to V_{IH}. An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address range that each sector occupies. A "sector address" consists of the address inputs required to uniquely select a sector. See the "Command Definitions" section for details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on I/O_7 - I/O_0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

I_{CC2} in the Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on I/O_7 - I/O_0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to each AC Characteristics section for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the $\overline{OE}$ input.

The device enters the CMOS standby mode when the $\overline{CE}$ pin is held at V_{CC} ± 0.5V. (Note that this is a more restricted voltage range than V_{IH}.) The device enters the TTL standby mode when $\overline{CE}$ is held at V_{IH}. The device requires the standard access time (tCE) before it is ready to read data. If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics tables represents the standby current specification.

Output Disable Mode

When the $\overline{OE}$ input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2 - Sector Addresses Table

Sector	A18	A17	A16	Address Range
SA0	0	0	0	00000h - 0FFFFh
SA1	0	0	1	10000h - 1FFFFh
SA2	0	1	0	20000h - 2FFFFh
SA3	0	1	1	30000h - 3FFFFh
SA4	1	0	0	40000h - 4FFFFh
SA5	1	0	1	50000h - 5FFFFh
SA6	1	1	0	60000h - 6FFFFh
SA7	1	1	1	70000h - 7FFFFh

Note: All sectors are 64 Kbytes in size.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on I/O_7 - I/O_0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5V to 12.5 V) on address pin A_9. Address pins A_6, A_1, and A_0 must be as shown in Table 3 below. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on I/O_7 - I/O_0.To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 3 - PY29F040 Autoselect Codes (High Voltage Method)

Description	A_{18}-A_{16}	A_{15}-A_{10}	A_9	A_8-A_7	A_6	A_5-A_2	A_1	A_0	Identifier Code on I/O_7-I/O_0
Manufacturer ID	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IL}	37h
Device ID	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IH}	86h
Sector Protection Verification	Sector Address	X	V_{ID}	X	V_{IL}	X	V_{IH}	V_{IL}	01h (protected)
									00h (unprotected)
Continuation ID	X	X	V_{ID}	X	V_{IL}	X	V_{IH}	V_{IH}	7Fh

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection must be implemented using programming equipment. The procedure requires a high voltage (V_{ID}) on address pin A_9 and the control pins. The device is shipped with all sectors unprotected. It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

Hardware Data Protection

The requirement of command unlocking sequence for programming or erasing provides data protection against inadvertent writes (refer to the Command Definitions table). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up transitions, or from system noise. The device is powered up to read array data to avoid accidentally writing data to the array.

Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{OE}$ =V_{IL}, $\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

If $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ during power up, the device does not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to reading array data on the initial power-up.

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. The Command Definitions table defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. All addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. All data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm. After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system must issue the reset command to re-enable the device for reading array data if I/O_5 goes high, or while in the autoselect mode. See the "Reset Command" section, next. See also "Requirements for Reading Array Data" in the "Device Bus Operations" section for more information. The Read Operations table provides the read parameters, and Read Operation Timings diagram shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command. The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data (also applies to autoselect during Erase Suspend).

If I/O_5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. This method is an alternative to that shown in the Autoselect Codes (High Voltage Method) table, which is intended for PROM programmers and requires V_{ID} on address bit A_9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code and another read cycle at XX03h retrieves the continuation code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in returns 01h if that sector is protected, or 00h if it is unprotected. Refer to the Sector Address tables for valid sector addresses.

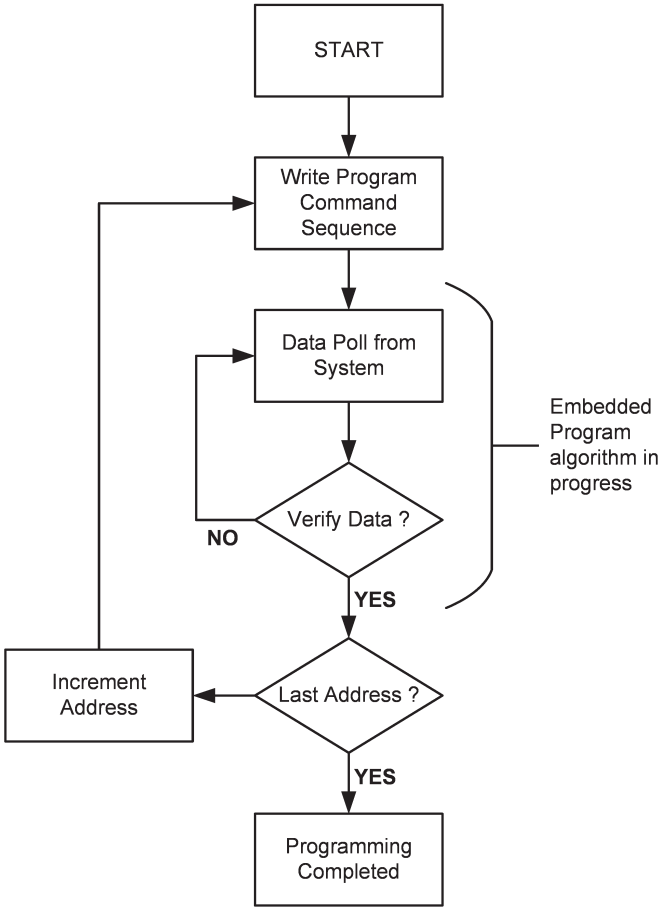
The system must write the reset command to exit the autoselect mode and return to reading array data.

Byte Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. The Command Definitions table shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using I/O_7 or I/O_6. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a "0" back to a "1 ". Attempting to do so may halt the operation and set I/O_5 to "1", or cause the $\overline{DATA}$ Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1"



Note: See the appropriate Command Definitions table for program command sequence

Figure 1. Program Operation

Chip Erase Command Sequence

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. The system can determine the status of the erase operation by using I/O_7, I/O_6, or I/O_2. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 2 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to the Chip/Sector Erase Operation Timings for timing waveforms.

Sector Erase Command Sequence

Sector erase is a six-bus-cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase timeout of 50µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50µs, the system need not monitor I/O_3. Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor I/O_3 to determine if the sector erase timer has timed out. (See the "I/O_3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final $\overline{WE}$ pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using I/O_7, I/O_6, or I/O_2. Refer to "Write Operation Status" for information on these status bits.

Figure 2 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50µs time-out period during the sector erase

command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't cares" when writing the Erase Suspend command.

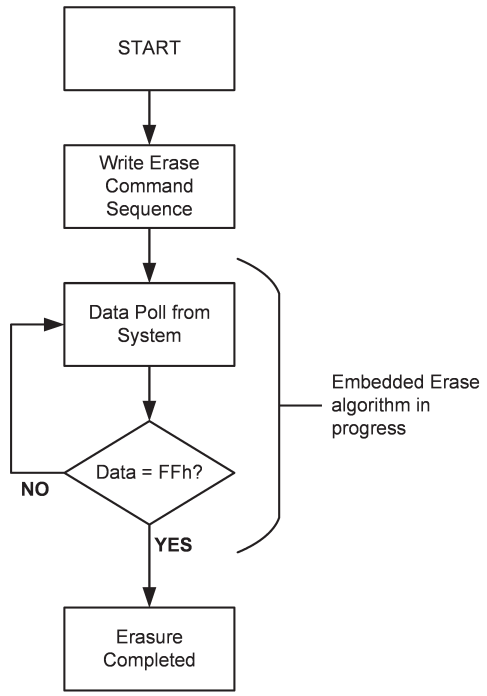
When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 30µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on I/O_7 - I/O_0. The system can use I/O_7, or I/O_6 and I/O_2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non- suspended sectors. The system can determine the status of the program operation using the I/O_7 or I/O_6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

The system must write the Erase Resume command (address bits are "don't care") to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.



Notes:
1. See the appropriate Command Definitions table for program command sequence.
2. See "I/O_3: Sector Erase Timer" for more information.

Figure 2. Erase Operation

Table 4 - PY29F040 Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2-4) First Addr	First Data	Second Addr	Second Data	Third Addr	Third Data	Fourth Addr	Fourth Data	Fifth Addr	Fifth Data	Sixth Addr	Sixth Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	37				
	Device ID	4	555	AA	2AA	55	555	90	X01	86				
	Continuation ID	4	555	AA	2AA	55	555	90	X03	7F				
	Sector Protect Verify (Note 8)	4	555	AA	2AA	55	555	90	SA X02	00				
										01				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 9)		1	XXX	B0										
Erase Resume (Note 10)		1	XXX	30										

Legend:
X = Don't Care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the failing edge of the $\overline{WE}$ or $\overline{CE}$ pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of $\overline{WE}$ or $\overline{CE}$ pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A_{18} - A_{16} select a unique sector.

Notes:
1. See Table 1 for description of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or autoselect data, all bus cycles are write operation.
4. Address bits A_{18} - A_{11} are don't cares for unlock and command cycles, unless SA or PA required.
5. No unlock or command cycles required when reading array data.
6. The Reset command is required to return to reading array data when device is in the autoselect mode, or if I/O_5 goes high (while the device is providing status data).
7. The fourth cycle of the autoselect command sequence is a read cycle.
8. The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.
9. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode.
10. The Erase Resume command is valid only during the Erase Suspend mode.

Write Operation Status

Several bits, I/O_2, I/O_3, I/O_5, I/O_6, and I/O_7, are provided in the PY29F040 to determine the status of a write operation. Table 5 and the following subsections describe the functions of these status bits. I/O_7, I/O_6 and I/O_2 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

I/O_7: $\overline{DATA}$ Polling

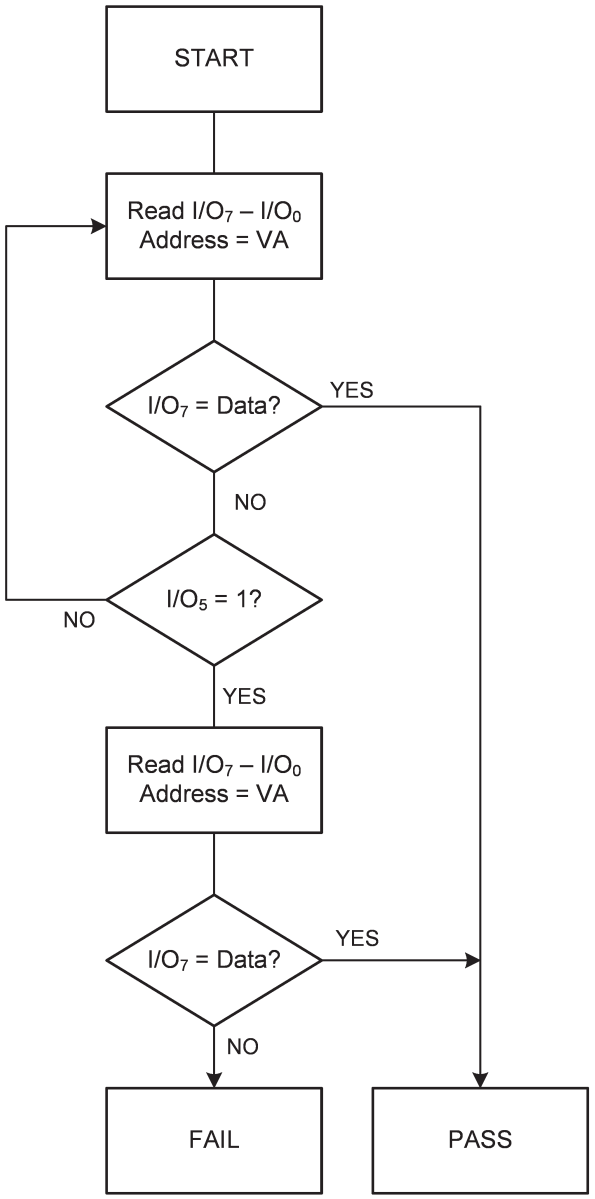
The $\overline{DATA}$ Polling bit, I/O_7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. $\overline{DATA}$ Polling is valid after the rising edge of the final $\overline{WE}$ pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on I/O_7 the complement of the datum programmed to I/O_7. This I/O_7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to I/O_7. The system must provide the program address to read valid status information on I/O_7. If a program address falls within a protected sector, $\overline{DATA}$ Polling on I/O_7 is active for approximately 2µs, then the device returns to reading array data.

During the Embedded Erase algorithm, $\overline{DATA}$ Polling produces a "0" on I/O_7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, $\overline{DATA}$ Polling produces a "1" on I/O_7.This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to "1"; prior to this, the device outputs the "complement," or "0." The system must provide an address within any of the sectors selected for erasure to read valid status information on I/O_7.

After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{DATA}$ Polling on I/O_7 is active for approximately 100µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects I/O_7 has changed from the complement to true data, it can read valid data at I/O_7 - I/O_0 on the following read cycles. This is because I/O_7 may change asynchronously with I/O_0 - I/O_6 while Output Enable ($\overline{OE}$) is asserted low. The $\overline{DATA}$ Polling Timings (During Embedded Algorithms) figure in the "AC Characteristics" section illustrates this. Table 5 shows the outputs for $\overline{DATA}$ Polling on I/O_7. Figure 3 shows the $\overline{DATA}$ Polling algorithm.



Note:
1. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.

2. I/O_7 should be rechecked even if I/O_5 = "1" because I/O_7 may change simultaneously with I/O_5.

Figure 3. $\overline{DATA}$ Polling Algorithm

I/O_6: Toggle Bit I

Toggle Bit I on I/O_6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause I/O_6 to toggle. (The system may use $\overline{OE}$ and $\overline{CE}$ to control the read cycles.) When the operation is complete, I/O_6 stops toggling. After an erase command sequence is written, if all sectors selected for erasing are protected, I/O_6 toggles for approximately 100µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use I/O_6 and I/O_2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), I/O_6 toggles. When the device enters the Erase Suspend mode, I/O_6 stops toggling. However, the system must also use I/O_2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use I/O_7 (see the subsection on " I/O_7 : $\overline{DATA}$ Polling").

If a program address falls within a protected sector, I/O_6 toggles for approximately 2µs after the program command sequence is written, then returns to reading array data.

I/O_6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

The Write Operation Status table shows the outputs for Toggle Bit I on I/O_6. Refer to Figure 4 for the toggle bit algorithm, and to the Toggle Bit Timings figure in the "AC Characteristics" section for the timing diagram. The I/O_2 vs. I/O_6 figure shows the differences between I/O_2 and I/O_6 in graphical form. See also the subsection on " I/O_2: Toggle Bit II".

I/O_2: Toggle Bit II

The "Toggle Bit II" on I/O_2, when used with I/O_6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence.

I/O_2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use $\overline{OE}$ and $\overline{CE}$ to control the read cycles.) But I/O_2 cannot distinguish whether the sector is actively erasing or is erase-suspended. I/O_6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 5 to compare outputs for I/O_2 and I/O_6.

Figure 4 shows the toggle bit algorithm in flowchart form, and the section " I/O_2: Toggle Bit II" explains the algorithm. See also the " I/O_6: Toggle Bit I" subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The I/O_2 vs. I/O_6 figure shows the differences between I/O_2 and I/O_6 in graphical form.

Reading Toggle Bits I/O_6, I/O_2

Refer to Figure 4 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read I/O_7 - I/O_0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on I/O_7 - I/O_0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of I/O_5 is high (see the section on I/O_5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as I/O_5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and I/O_5 has not gone high. The system may continue to monitor the toggle bit and I/O_5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 4).

I/O_5: Exceeded Timing Limits

I/O_5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions I/O_5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed.

The I/O_5 failure condition may appear if the system tries to program a "1 "to a location that is previously programmed to "0." Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, I/O_5 produces a "1."

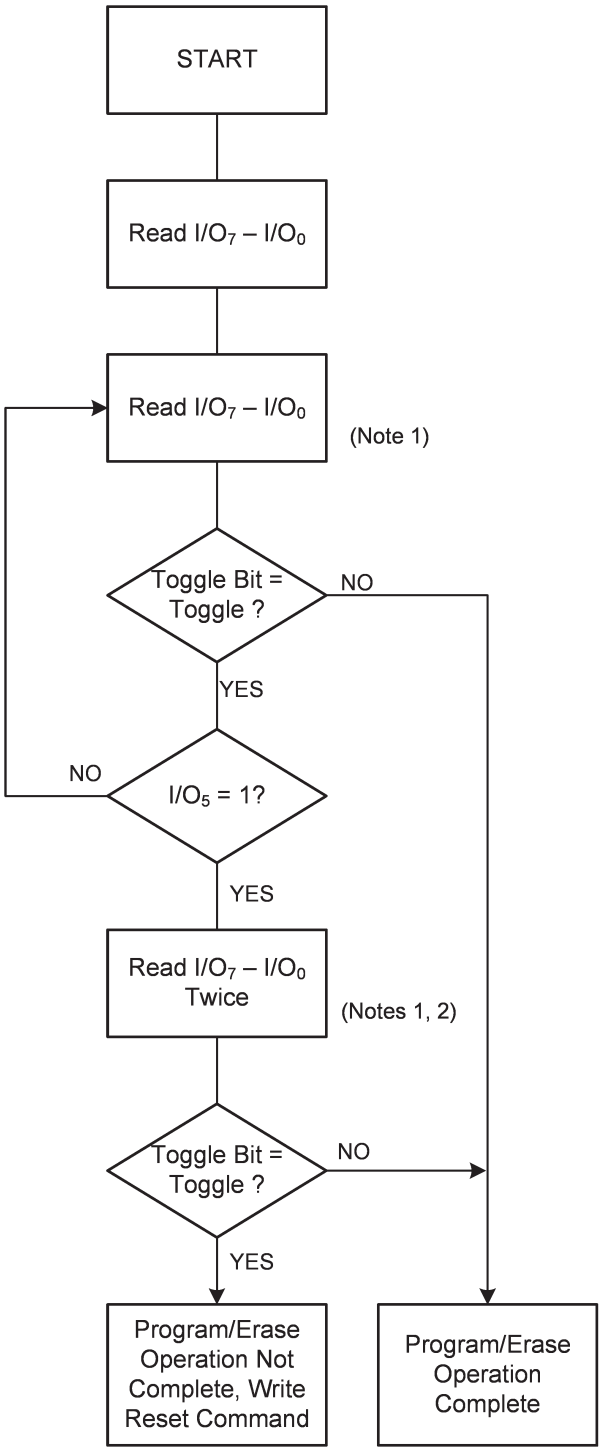
Under both these conditions, the system must issue the reset command to return the device to reading array data.

I/O_3: Sector Erase Timer

After writing a sector erase command sequence, the sys-

tem may read I/O_3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, I/O_3 switches from "0" to "1." The system may ignore I/O_3 if the system can guarantee that the time between additional sector erase commands will always be less than 50µs. See also the "Sector Erase Command Sequence" section.

After the sector erase command sequence is written, the system should read the status on I/O_7 ($\overline{DATA}$ Polling) or I/O_6 (Toggle Bit 1) to ensure the device has accepted the command sequence, and then read I/O_3. If I/O_3 is "1", the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If I/O_3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of I/O_3 prior to and following each subsequent sector erase command. If I/O_3 is high on the second status check, the last command might not have been accepted. Table 5 shows the outputs for I/O_3.



Note:
1. Read toggle bit twice to determine whether or not it is toggling. See text
2. Recheck toggle bit because it may stop toggling as I/O_5 changes to "1". See text.

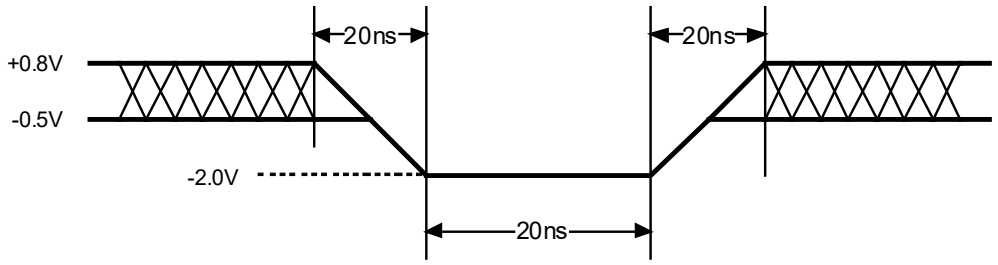
Figure 4. Toggle Bit Algorithm

Table 5 - Write Operation Status

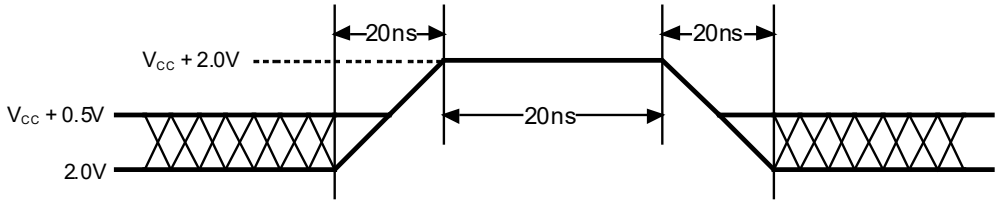
Operation		I/O_7 (Note 1)	I/O_6	I/O_5 (Note 2)	I/O_3	I/O_2 (Note 1)
Standard Mode	Embedded Program Algorithm	$\overline{I/O_7}$	Toggle	0	N/A	No toggle
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle
	Reading within Non-Erase Suspend Sector	Data	Data	Data	Data	Data
	Erase-Suspend-Program	$\overline{I/O_7}$	Toggle	0	N/A	N/A

Notes:
1. I/O_7 and I/O_2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. I/O_5 switches to "1" when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "I/O_5: Exceeded Timing Limits" for more information.

Maximum Negative Input Overshoot



Maximum Positive Input Overshoot



DC Characteristics

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min.	Typ.	Max.	Unit
I_{LI}	Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}. $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A_9 Leakage Current	$V_{CC} = V_{CC}$ Max, A_9 = 12.5V			100	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}. $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		20	30	mA
I_{CC2}	V_{CC} Active Write (Program/Erase) Current (Notes 2, 3, 4)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	40	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	$\overline{CE} = V_{IH}$		0.4	1.0	mA
V_{IL}	Input Low Level		-0.5		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.25V	10.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -2.5mA, $V_{CC} = V_{CC}$ Min	2.4			V

CMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min.	Typ.	Max.	Unit
I_{LI}	Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}. $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A_9 Leakage Current	$V_{CC} = V_{CC}$ Max, A_9 = 12.5V			100	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}. $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		20	30	mA
I_{CC2}	V_{CC} Active Write (Program/Erase) Current (Notes 2, 3, 4)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	40	mA
I_{CC3}	V_{CC} Standby Current (Notes 2, 5)	$\overline{CE} = V_{CC}$ ± 0.5V		1	5	µA
V_{IL}	Input Low Level		-0.5		0.8	V
V_{IH}	Input High Level		0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.25V	10.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.5mA, $V_{CC} = V_{CC}$ Min	0.85 x V_{CC}			V
V_{OH2}		I_{OH} = -100µA, $V_{CC} = V_{CC}$ Min	V_{CC} - 0.4			

Notes:
1. The I_{CC} current listed includes both the DC operation current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$ Max.
3. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
4. Not 100% tested.
5. For CMOS mode only, I_{CC3} = 20µA max at extended temperatures (> +85°C).

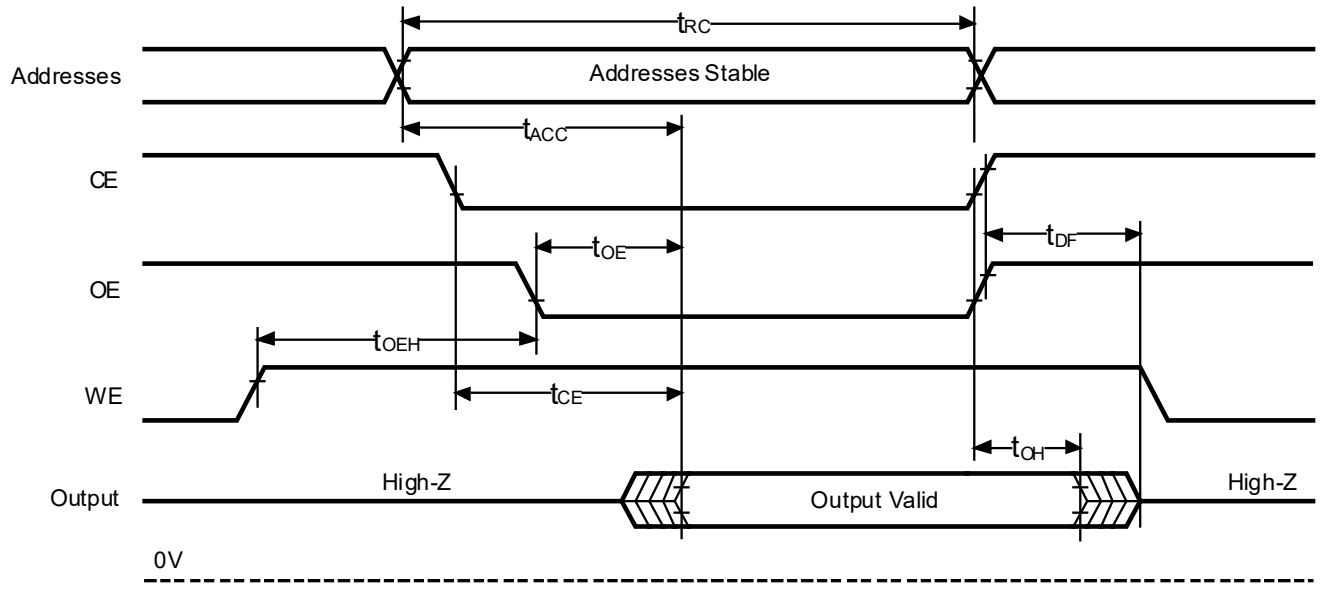
AC Characteristics

Read Only Operations

Parameter Symbols JEDEC	Parameter Symbols STD	Description		Test Setup		Speed -55	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 2)			Min	55	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	55	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		$\overline{OE} = V_{IL}$	Max	55	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	ns
	t_{OEH}	Output Enable Hold Time (Note 2)	Read		Min	0	ns
			Toggle and $\overline{DATA}$ Polling		Min	10	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 1, 2)			Max	18	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1, 2)			Max	18	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First			Min	0	ns

Notes:
1. Output driver disable time.
2. Not 100% tested.

Timing Waveforms for Read Only Operation



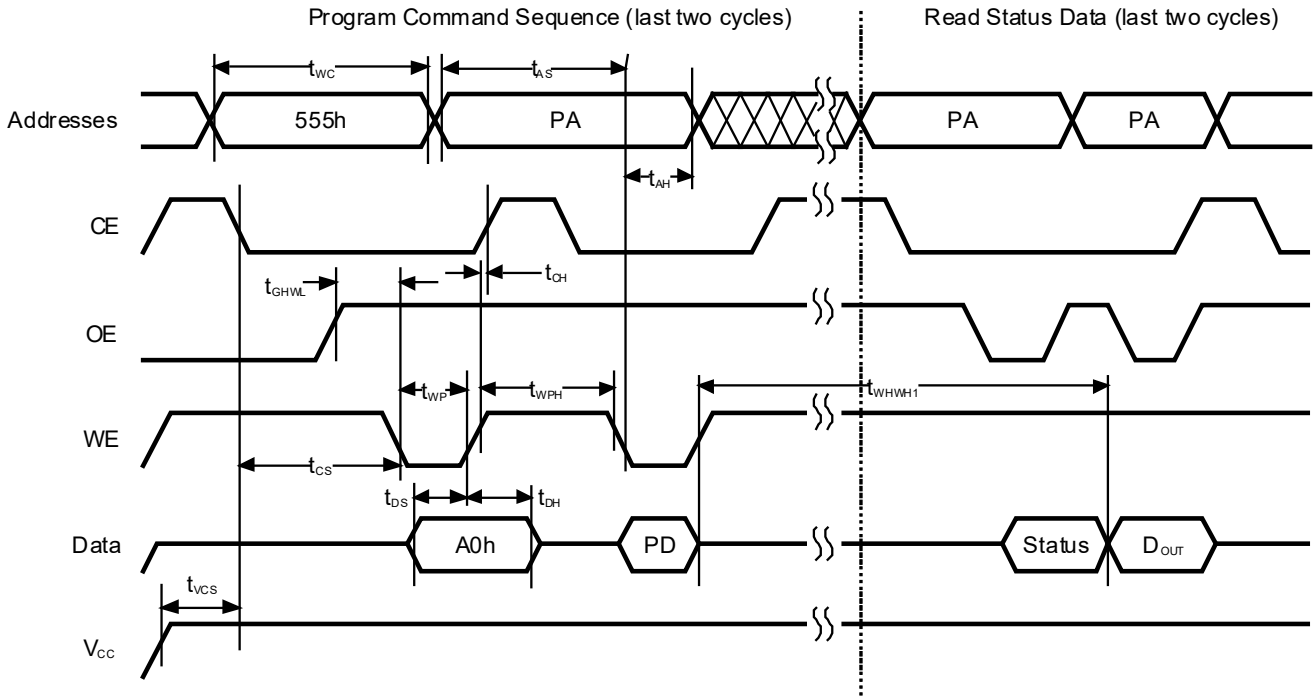
AC Characteristics

Erase and Program Operations

Parameter Symbols		Description		Speed	Unit
JEDEC	Std			-55	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	55	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	25	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ high to $\overline{WE}$ low)	Min	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	Min	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	Min	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	30	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20	ns
			Max	50	µs
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2)	Typ	35	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	2	sec
	t_{VCS}	VCC Set Up Time (Note 1)	Min	50	µs

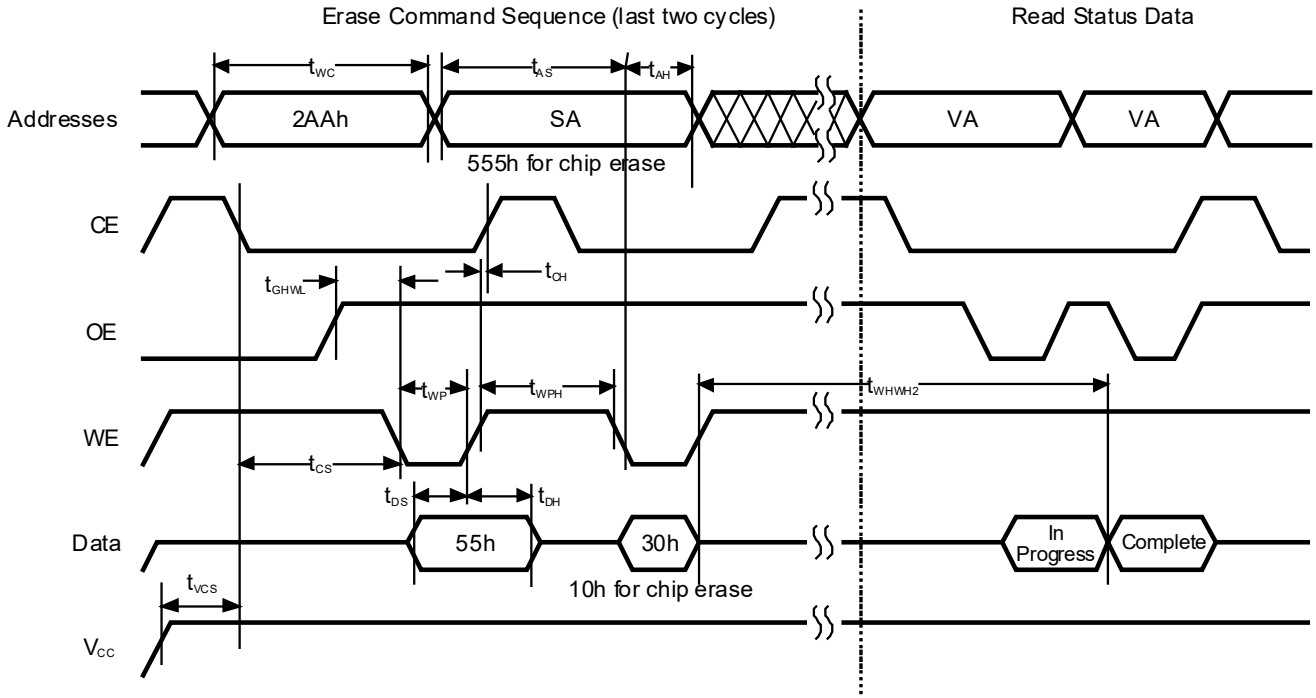
Notes:
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

Timing Waveforms for Program Operation



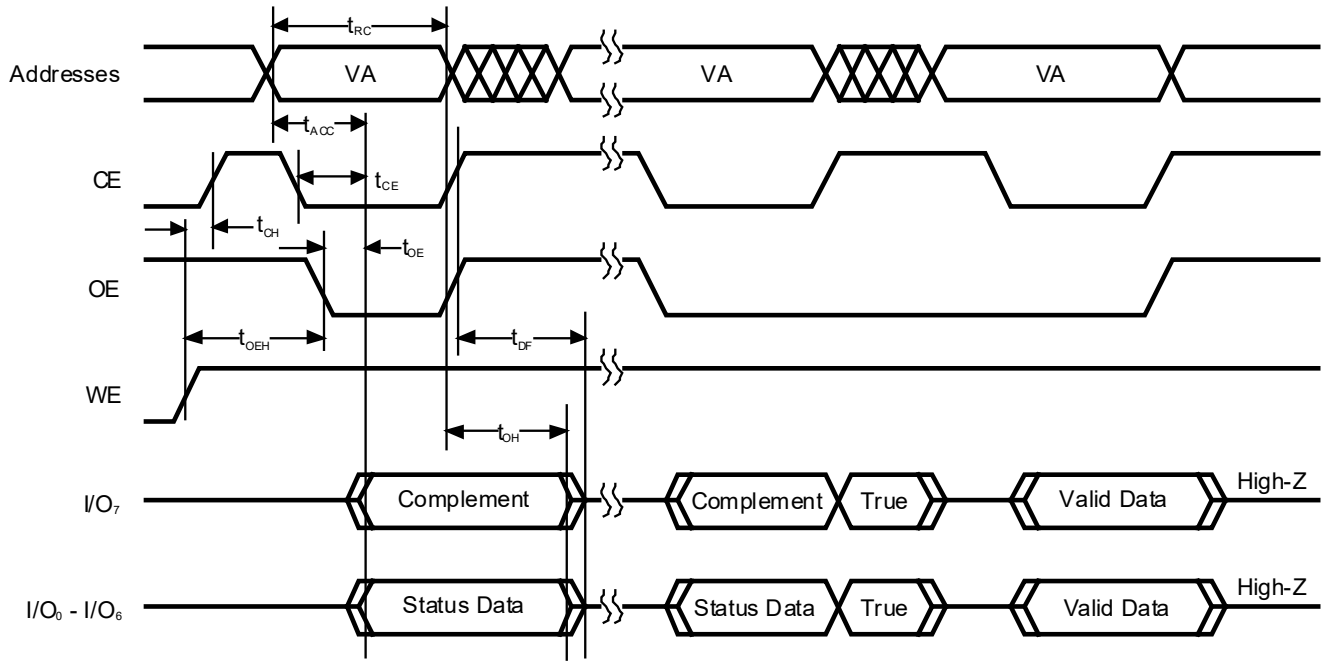
Note:
PA = Program Address, PD = Program Data, D_{OUT} is the true data at the program address.

Timing Waveforms for Chip/Sector Erase Operation



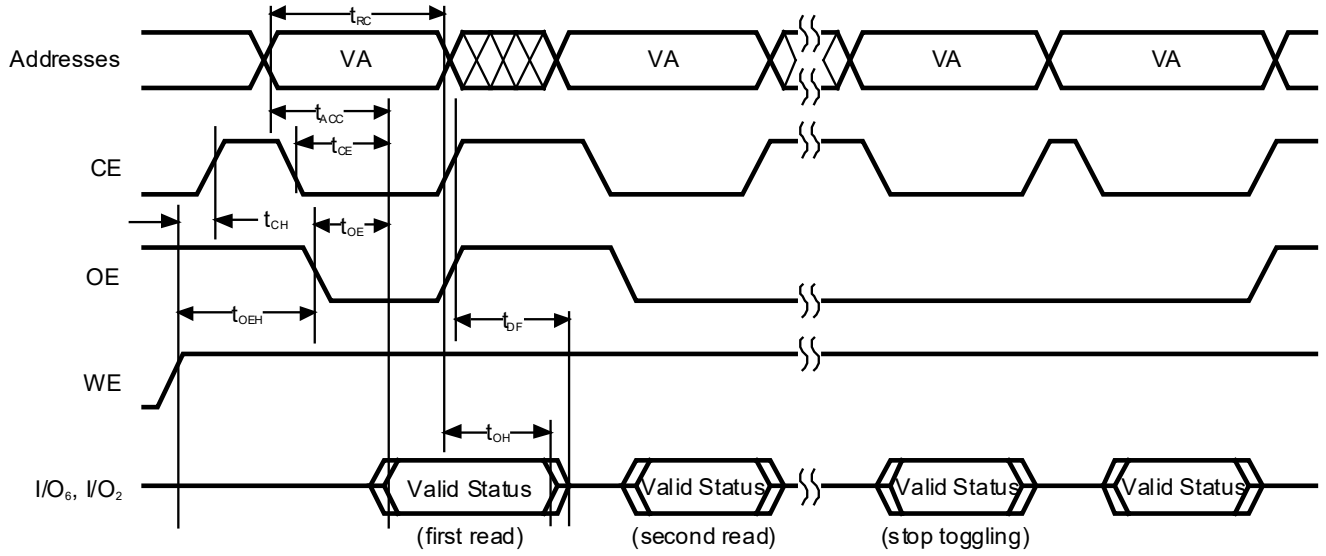
Note:
SA = Sector Address. VA = Valid Address for reading status data

Timing Waveforms for $\overline{\text{DATA}}$ Polling (During Embedded Algorithms)



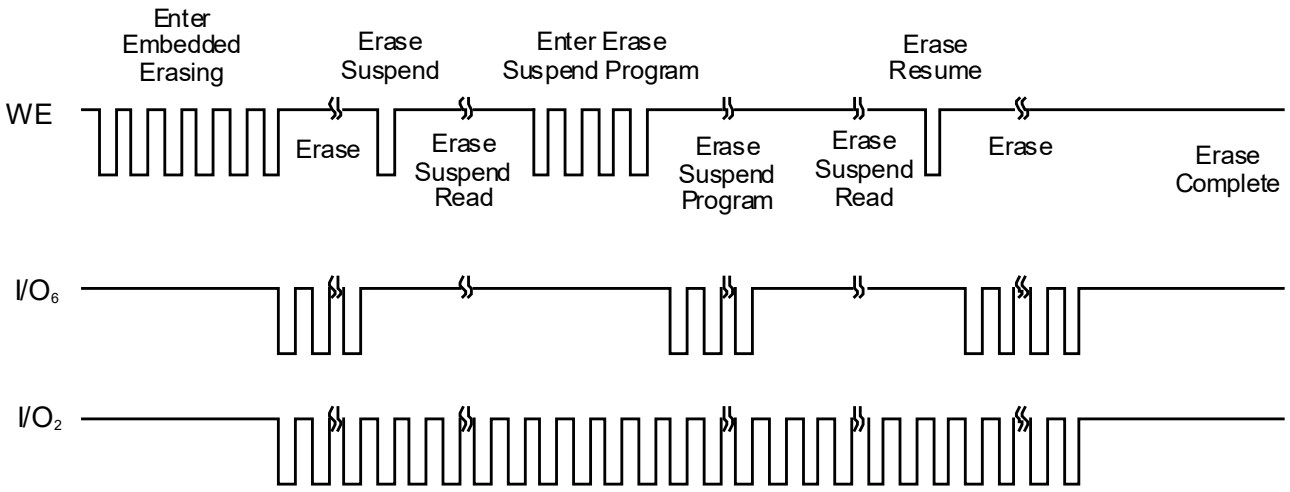
Note:
VA = Valid Address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Timing Waveforms for Toggle Bit (During Embedded Algorithms)



Note:
VA = Valid Address; not required for I/O_6. Illustration shows first two status cycles after command sequence, last status read cycle, and array data read cycle.

Timing Waveforms for I/O_2 vs. I/O_6



Note:
Both I/O_6 and I/O_2 toggle with $\overline{OE}$ or $\overline{CE}$. See the text on I/O_6 and I/O_2 in the section "Write Operation Status" for more information.

AC Characteristics

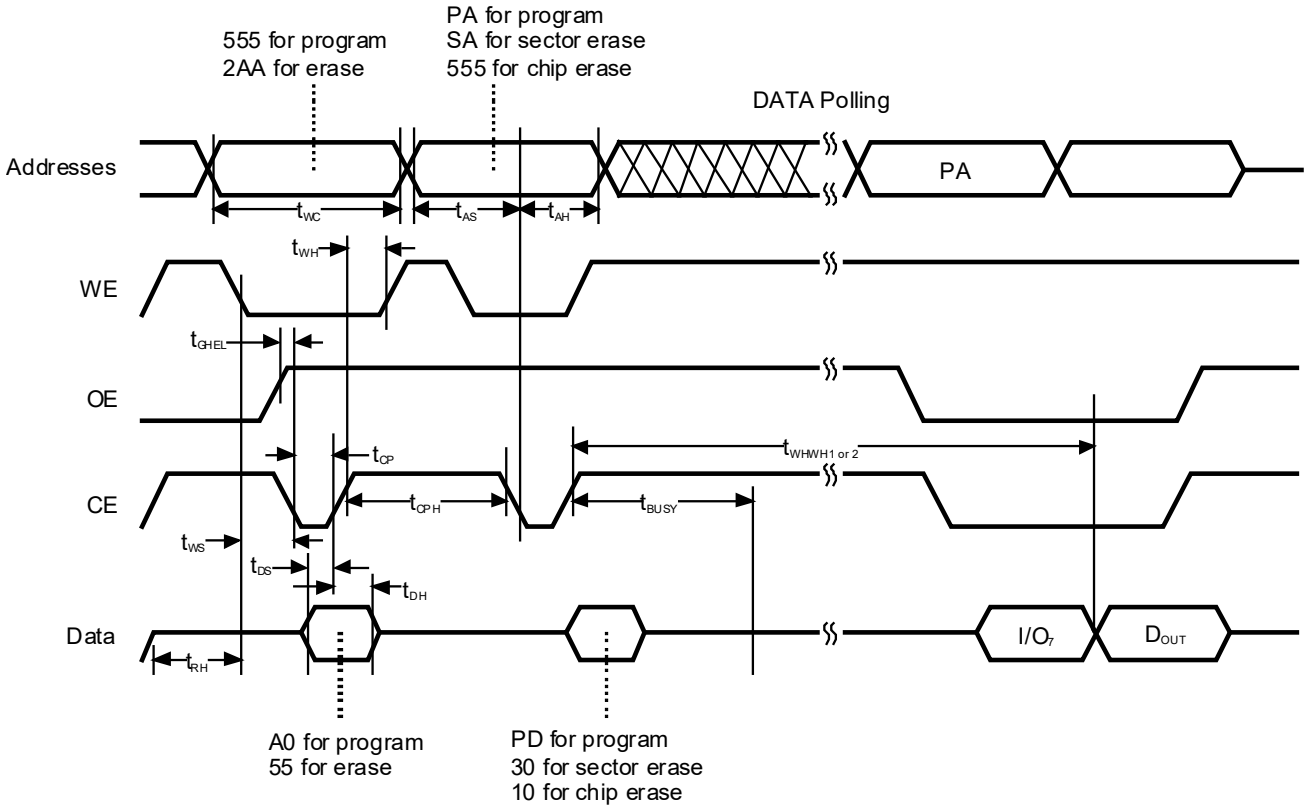
Erase and Program Operations

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols		Description		Speed	Unit
JEDEC	Std			-55	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	55	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	40	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	25	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	Min	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time	Min	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time	Min	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min	30	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High	Min	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2)	Typ	35	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	2	sec

Notes:
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

Timing Waveforms for Alternate $\overline{CE}$ Controlled Write Operation



Note:
1. PA = Program Address, PD = Program Data, SA = Sector Address, $\overline{I/O_7}$ = Complement of Data Input, D_{OUT} = Array Data.
2. Figure indicates the last two bus cycles of the command sequence.

Erase and Programming Performance

Parameter	Typ. (Note 1)	Max. (Note 2)	Unit	Comments
Sector Erase Time	2	8	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	16	64	sec	
Byte Programming Time	35	300	µs	Excludes system-level overhead (Note 5)
Chip Programming Time (Note 3)	3.6	10.8	sec	

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 5.0V V_{CC}, 10,000 cycles. Additionally, programming typically assumes checkerboard pattern.
2. Under worst case conditions of 90°C, V_{CC} = 4.5V (4.75V for -55), 100,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum byte programming time listed. If the maximum byte program time given is exceeded, only then does the device set I/O_5 = 1. See the section on I/O_5 for further information.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the four-bus-cycle command sequence for programming. See Table 4 for further information on command definitions.
6. The device has a guaranteed minimum erase and program cycle endurance of 100,000 cycles.

Latch-up Characteristics

Description	Min	Max
Input Voltage with respect to V_{SS} on all I/O pins	-1.0V	V_{CC} + 1.0V
V_{CC} Current	-100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0V, one pin at a time.

PLCC Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{PP} = 0	8	12	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0MHz

Data Retention

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

Test Conditions

Table 6 - Test Specifications

Test Condition	-55	All Others	Unit
Output Load	1 TTL Gate		
Output Load Capacitance, CL (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5	20	ns
Input Pulse LEvels	0.0 - 3.0	0.45 - 2.4	V
Input timing measurement reference levels	1.5	0.8, 2.0	V
Output timing measurement reference levels	1.5	0.8, 2.0	V

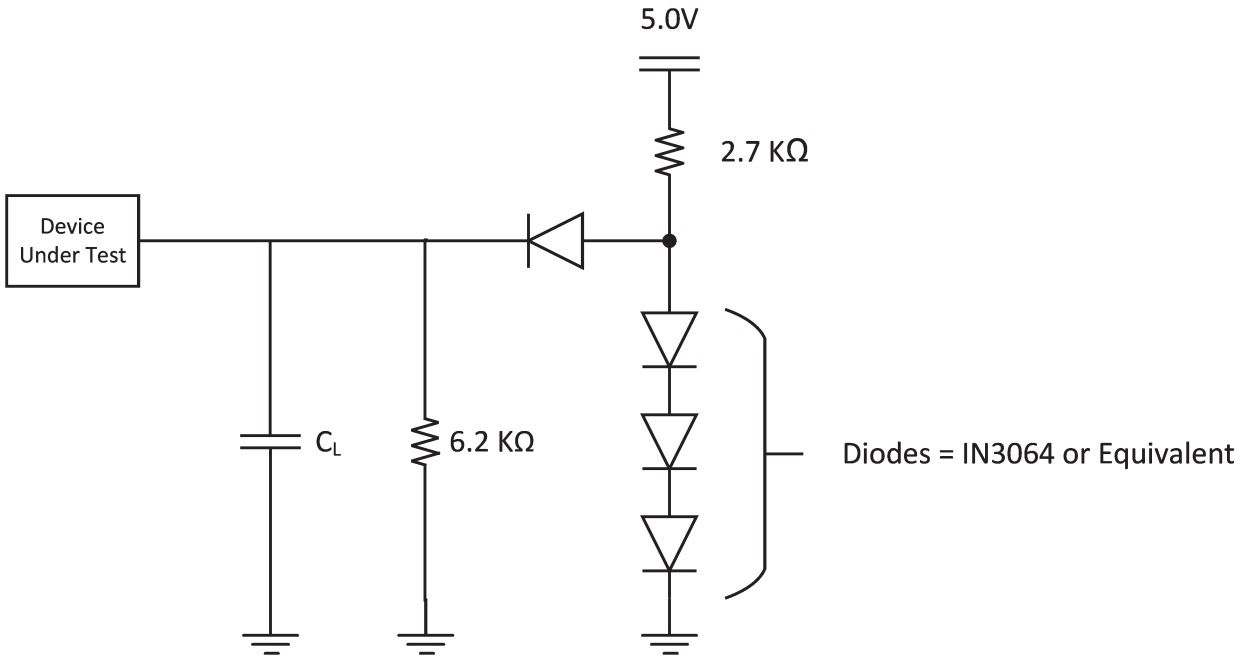
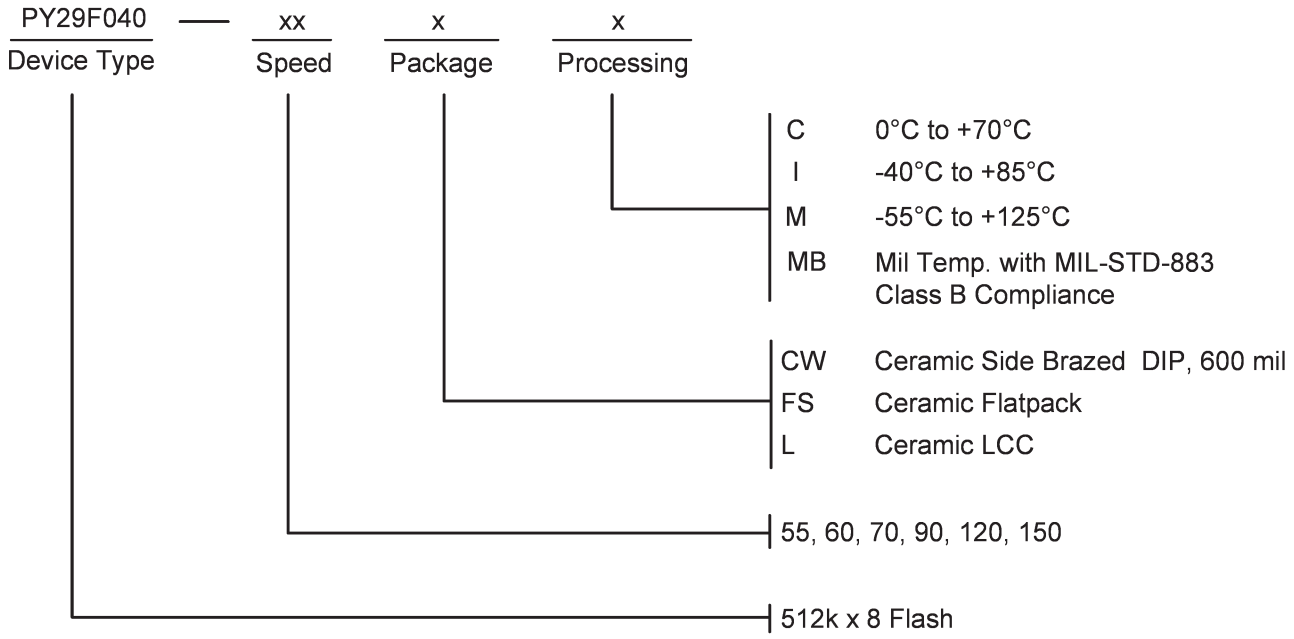


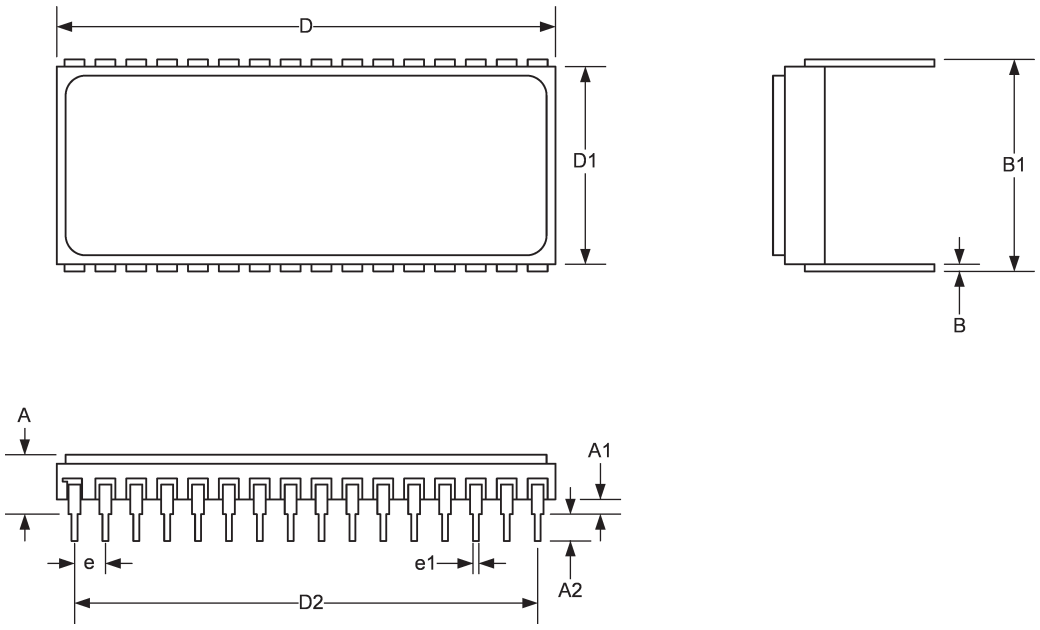
Figure 7. Test Setup

ORDERING INFORMATION



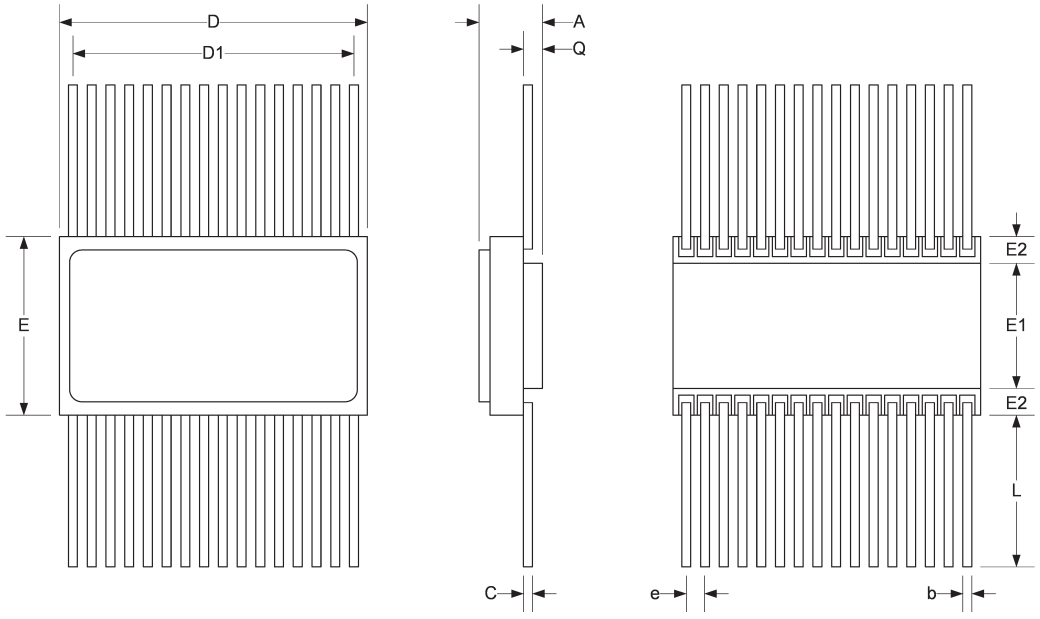
Pkg #	CW	
# Pins	32 (600 mil)	
Symbol	**Min**	**Max**
A	0.140	0.200
A1	0.019	0.047
A2	0.125	0.193
B	0.009	0.012
B1	0.588	0.617
D	1.654	1.686
D1	0.580	0.605
D2	1.492	1.508
e	0.100 BSC	
e1	0.016	0.020

SIDE-BRAZED DUAL IN-LINE PACKAGE



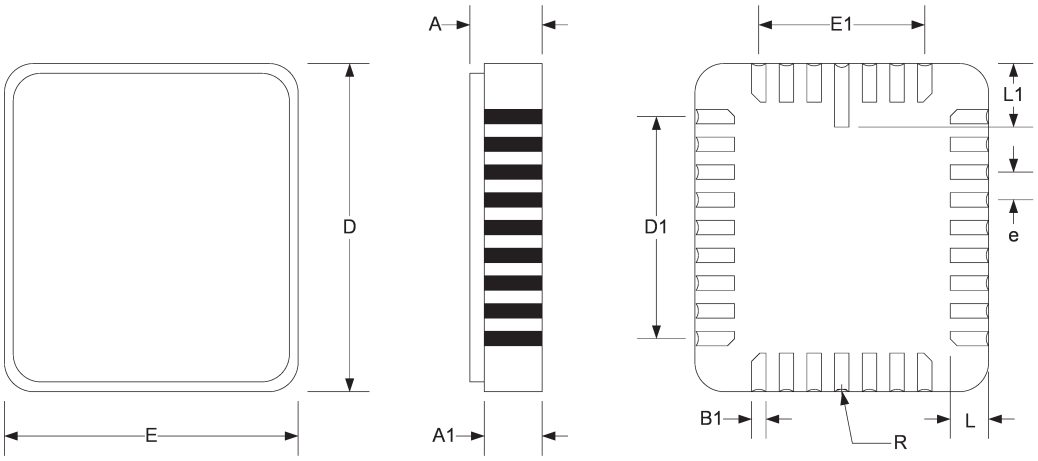
Pkg #	FS	
# Pins	32	
Symbol	**Min**	**Max**
A	—	0.125
b	0.015	0.019
C	0.004	0.007
D	0.810	0.830
D1	0.750 TYP	
E	0.405	0.415
E1	0.305	0.315
E2	0.050 TYP	
e	0.050 TYP	
L	0.380	0.420
Q	0.022	0.028

SOLDER SEAL FLATPACK



Pkg #	L	
# Pins	32	
Symbol	**Min**	**Max**
A	0.060	0.080
A1	0.040	0.050
B1	0.022	0.028
D	0.540	0.560
D1	0.390	0.410
E	0.442	0.458
E1	0.290	0.310
e	0.045	0.055
L	0.045	0.055
L1	0.075	0.095
R	0.004	0.014

LEADLESS CHIP CARRIER



REVISIONS

DOCUMENT NUMBER	PY29F040
DOCUMENT TITLE	PY29F040 - 512K x 8 FLASH

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Dec 2025	VM	New Data Sheet